DIC120
Programmable I/O Module

Features

- System bus: 8-bit ISA bus
- Digital I/O: 96 (DIC120-01) or 48 (DIC120-02) digital I/O channels with logical signal levels (CMOS, TTL)
- Support of timers/pulse counters
- Power consumption: +5 V ± 5%, no more than 340 mA
- Operating temperature range: from –40°C to +85°C
- Dimensions: no more than 125 mm × 115 mm
- Supported OS: FDOS, FreeDOS, Windows XP (Embedded), Linux 2.6

Overview

The module is implemented in MicroPC standard and is designed for input/output of 96 or 48 signals with CMOS logical levels, TTL or extension of system resources (e.g. support of additional system timers or acceleration of logical and arithmetic operations). The module can also be sued for measurement of frequency (duration) and signal phases, performing calculation and timing operations, generation of PWM-signals, conversion of codes, generation of control timing diagram and event hardware interrupts at inputs.

DIC120 is compatible with DIC110 module in terms of hardware and software.

Technical Specifications

System bus
- 8-bit ISA bus

Digital I/O
- 96 (DIC120-01) or 48 (DIC120-02) digital I/O channels with logical signal levels (CMOS, TTL)
- Measurement of frequency (up to 50 MHz) and signal phases on any channel
- Support of timers/ pulse counters
- Generation of frequency and PWM signals on any channel
- Conversion of codes on any channel
- Generation of control timing diagrams (not using system resources)
- Generation of event hardware interrupts at inputs
- Programmable time interval of de-bouncing for inputs
- Separate FPGA matrices with Flash-memory for storing configurations (firmware upgrades), 4 for DIC120-01, 2 for DIC120-02
- Ability to develop proprietary FPGA configurations (firmware upgrades)

Control capabilities
- Module addressing (legacy - same as with DIC110, index – address port, data port)
- Programming of interruptions
- Module (code of FPGA-matrix circuits) identification
- Programmability of module's circuit in the system (ISP)

Supported OS
- FDOS, FreeDOS
- Windows XP (Embedded)
- Linux 2.6

Power
- Power consumption:
  +5 V ± 5%, no more than 340 mA

Environmental
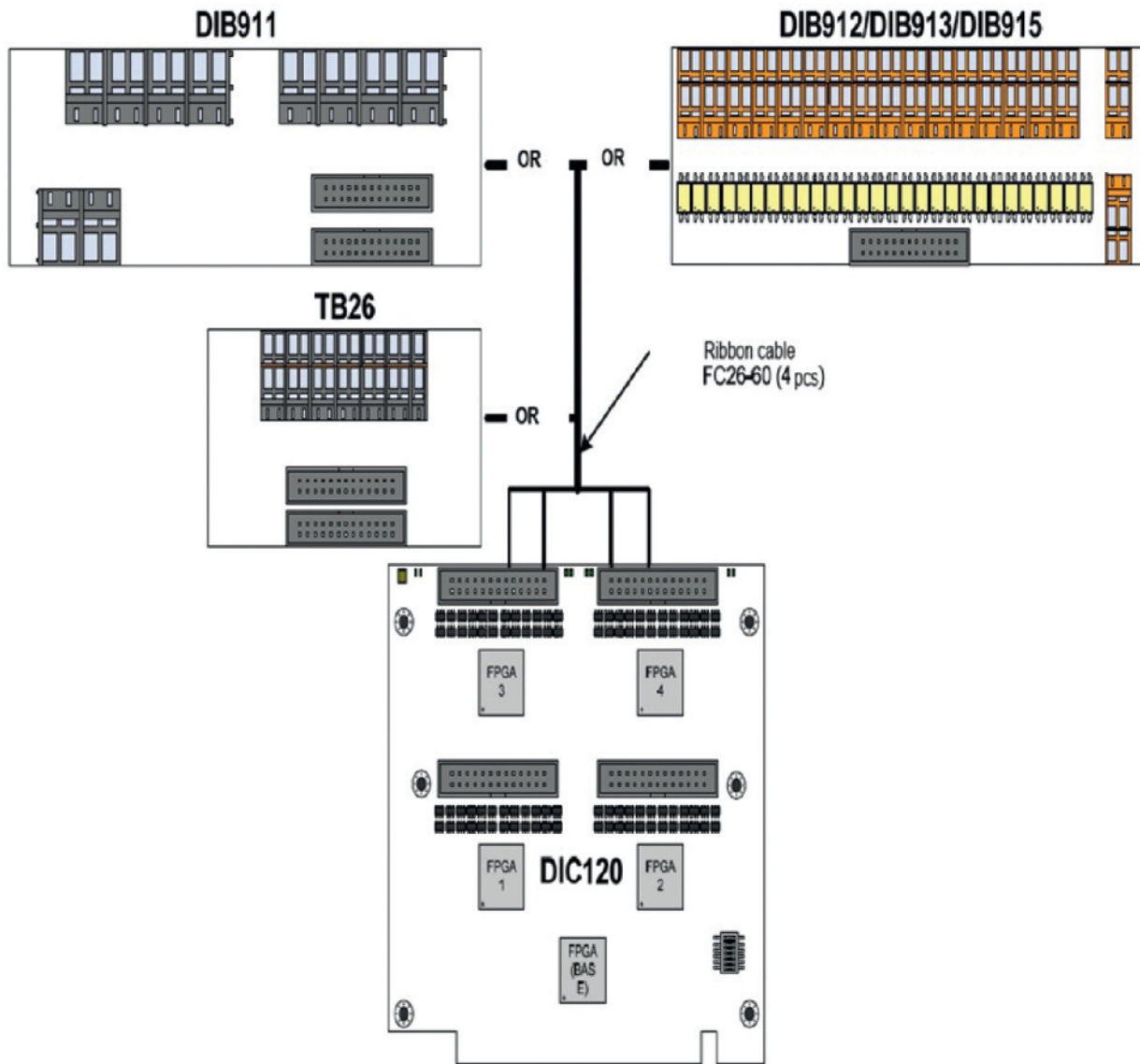- Operating temperature range:
  from –40°C to + 85°C

Mechanical
- Dimensions:
  no more than 125 mm × 115 mm

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Board Layout

DIB911

DIB912/DIB913/DIB915

TB26

OR

OR

OR

Ribbon cable
FC26-60 (4 pcs)

FPGA 3

FPGA 4

FPGA 1

DIC120

FPGA 2

FPGA (BASE)

Ordering Information

DIC120 Configuration

DIC120 - 01

Configurations

01	96 I/O channels
02	48 I/O channels

Additional accessories

ACS00002 (FC26-60) – flat ribbon cable, 26 threads, IDC connectors, 0.6 m (2 ft)
DIB91101 (TBR8) – relay switching module, 8 channels
DIB91201 (TBI 24/0C-1), DIB91202 (TBI 24/0C-2), DIB91203 (TBI 24/0C-3) – isolated digital input terminal boards, 24 channels
DIB91301 (TBI 0/24C) – isolated digital output terminal board, 24 channels
DIB91501 (TBI 16/8C-1), DIB91502 (TBI 16/8C-2), DIB91503 (TBI 16/8C-3) – isolated digital I/O terminal boards (16 inputs, 8 outputs)
TIB96501 (TB26) – terminal board, 26 contacts

Versions of supported FPGA-configurations by the time the product has been launched to serial production:

t00 – 4x 16-bit timers/counters;
x00 – 2x 12-channel high-precision frequency meters;
p55 – 24-channel I/O port (8255 microchip emulator mode 0);
q00 – 8x frequency generators;
n02 – 4x PWM signal conditioners.

Future versions of supported FPGA configurations:

f01 – 4x 16-bit phasing tester;
c00 – Counters with de-bouncing digital inputs;
n03 – Digital-frequency interface;
n04 – Event interrupt conditioner with programmable de-bouncing function;
q02 – 6x PWM signal conditioners;
x01 – 2x high-precision extended range frequency meters;
x02 – 3x 8-channel averaging frequency meters;
x11 – 8x frequency meters in the range 0.8–25 KHz;
x12 – 8x frequency meters in the range 0.4–500 KHz.

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